Midterm Exam

(October 15th @ 7:30 pm)
Presentation and clarity are very important! Show your procedure!

PROBLEM 1 (20 PTS)

- Compute the result of the following operations. The operands are signed fixed-point numbers. The result must be a signed fixed point number. For the division, use $x = 5$ fractional bits.

1.001001 + 1.001	1001.0101 – 1.010101	0.01001 + 01.11111
1.01101 × 01.011	1.011 × 1.0101	10.10010 ÷ 0.101

PROBLEM 2 (30 PTS)

- Calculate the result (provide the 32-bit result) of the following operations with single floating point numbers. Truncate the results when required. When doing fixed-point division, use $x = 4$ fractional bits.

✓ C2FA8000 + 40E00000	✓ D0DA8000 – 50FA8000	✓ 80400000 × FAB80000	✓ FB380000 ÷ 48C00000

PROBLEM 3 (13 PTS)

- Convert the following signed fixed point numbers in format [12 8] to the dual fixed point format 12_8_4.

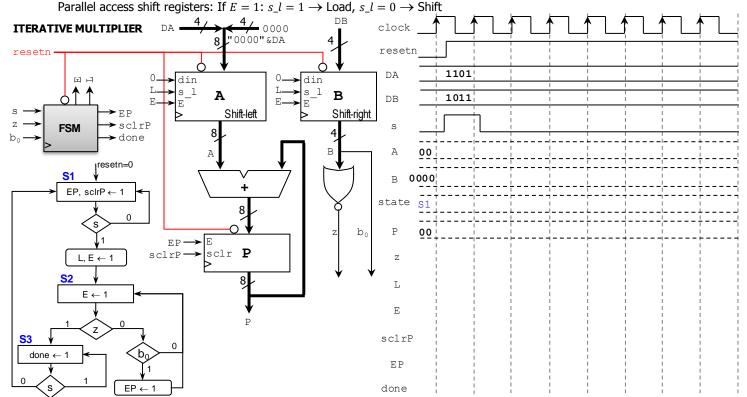| FX	A.CD	F.EA	8.CA	1.CA
DFX				

PROBLEM 4 (22 PTS)

- Calculate the result of the following operations where the numbers are represented in dual fixed-point arithmetic. Note that the results must be in the same format. Include an overflow bit when necessary.

DFX Format 12_6_4	Result	Overflow		Result	overflow
C2A + C0B			FBA–073		
ACD + B98			F33–4BF		

PROBLEM 5 (15 PTS)

- Complete the timing diagram of the following iterative unsigned multiplier ($N = 4, M = 4$).
  Register: $sclr$: synchronous clear. Here, if $sclr = E = 1$, the register contents are initialized to 0.

  Parallel access shift registers: If $E = 1$: $s\_l = 1 \rightarrow$ Load, $s\_l = 0 \rightarrow$ Shift